# FH1

**High Dynamic Range FET**

The Communications Edge ™

*Product Information*

## Product Features

- 50 – 3000 MHz
- Low Noise Figure
- 18 dB Gain
- +42 dBm OIP3
- +21 dBm P1dB
- Single or Dual Supply Operation
- Lead-free/Green/RoHS-compliant SOT-89 Package
- MTTF > 100 years

## Applications

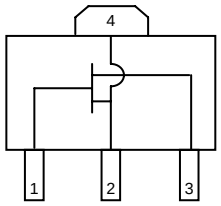
- Mobile Infrastructure
- CATV / DBS
- W-LAN / ISM
- Defense / Homeland Security

## Product Description

The FH1 is a high dynamic range FET packaged in a low-cost surface-mount package. The combination of low noise figure and high output IP3 at the same bias point makes it ideal for receiver and transmitter applications. The device combines dependable performance with superb quality to maintain MTTF values exceeding 100 years at mounting temperatures of +85°C. The FH1 is available in both the standard SOT-89 package and the environmentally-friendly lead-free/green/RoHS-compliant SOT-89 package.

The device utilizes a high reliability GaAs MESFET technology and is targeted for applications where high linearity is required. It is well suited for various current and next generation wireless technologies such as GPRS, GSM, CDMA, and W-CDMA. In addition, the FH1 will work for other applications within the 50 to 3000 MHz frequency range such as fixed wireless.

## Functional Diagram




| Function | Pin No. |
|---|---|
| Gate | 1 |
| Drain | 3 |
| Source | 2, 4 |

## Specifications (1)

| DC Electrical Parameter | Units | Min | Typ | Max |
|---|---|---|---|---|
| Saturated Drain Current, Idss (2) | mA | 100 | 140 | 170 |
| Transconductance, Gm | mS | | 120 | |
| Pinch-off Voltage, Vp (3) | V | -3 | -1.5 | |

| RF Parameter | Units | Min | Typ | Max |
|---|---|---|---|---|
| Operational Bandwidth | MHz | | 50 – 3000 | |
| Test Frequency | MHz | | 800 | |
| Small-signal Gain, Gss | dB | 17 | 18 | |
| Max Stable Gain, Gmsg | dB | | 23 | |
| Output IP3 (4) | dBm | +38 | +42 | |
| P1dB | dBm | | +21 | |
| Minimum Noise Figure (5) | dB | | 0.77 | |
| Drain Bias | V | | +5 | |
| Gate Bias | V | | 0 | |

1. DC and RF parameters are measured under the following conditions unless otherwise noted: 25°C with Vds = 5V, Vgs = 0V, in a 50 Ω system.
2. Idss is measured with Vgs = 0V.
3. Pinch-off voltage is measured with Ids = 0.6 mA.
4. 3OIP measured with two tones at an output power of +5 dBm/tone separated by 10 MHz. The suppression on the largest IM3 product is used to calculate the 3OIP using a 2:1 rule.
5. The minimum noise figure has $\Gamma_S = \Gamma_L = \Gamma_{OPT}$.

## Typical Performance (6)

| Parameter | Units | Typical | | |
|---|---|---|---|---|
| Frequency | MHz | 900 | 1960 | 2140 |
| S21 | dB | 19 | 16.5 | 16.5 |
| S11 | dB | -11 | -20 | -22 |
| S22 | dB | -10 | -9 | -9 |
| Output P1dB | dBm | +42 | +40 | +40 |
| Output IP3 (4) | dBm | +21.8 | +22.1 | +22.1 |
| Noise Figure | dB | 2.7 | 3.1 | 3.0 |
| Drain Bias | | 5V @ 140mA | | |
| Gate Voltage | V | 0 | | |

6. The device requires appropriate matching to become unconditionally stable. Parameters reflect performance in an appropriate application circuit.

## Absolute Maximum Rating

| Parameter | Rating |
|---|---|
| Operating Case Temperature | -40 to +85 °C |
| Storage Temperature | -55 to +150 °C |
| Drain to Source Voltage | +6 V |
| Gate to Source Voltage | -6 V |
| Gate Current | 4.5 mA |
| RF Input Power (continuous) | 4 dB above Input P1dB |
| Junction Temperature | +220 °C |

Operation of this device above any of these parameters may cause permanent damage.

## Ordering Information

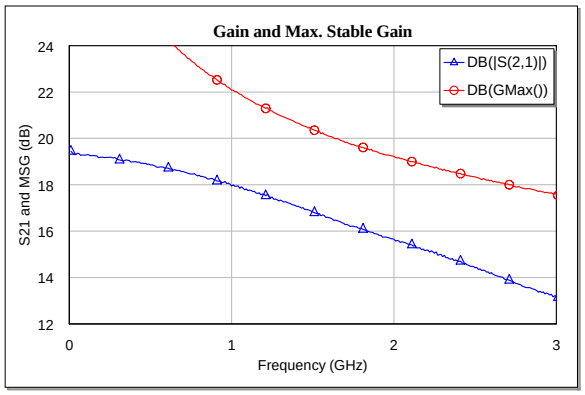
| Part No. | Description |
|---|---|
| FH1* | High Dynamic Range FET (lead-tin SOT-89 package) |
| FH1-G | High Dynamic Range FET (lead-free/green/RoHS-compliant SOT-89 package) |

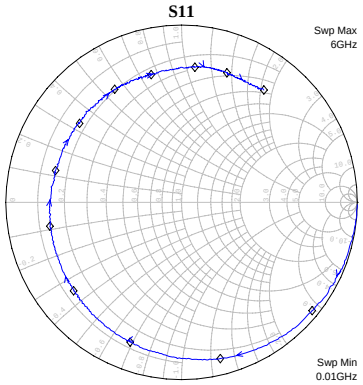
* This package is being phased out in favor of the green package type which is backwards compatible for existing designs. Refer to Product Change Notification WJPCN06MAY05TC1 on the WJ website.

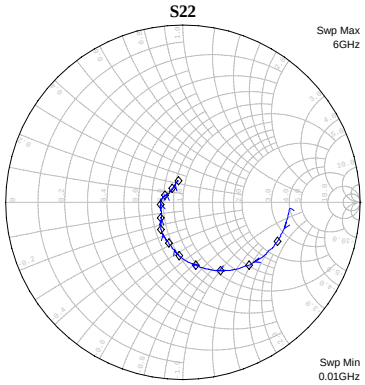
Specifications and information are subject to change without notice.

# Typical Device Data

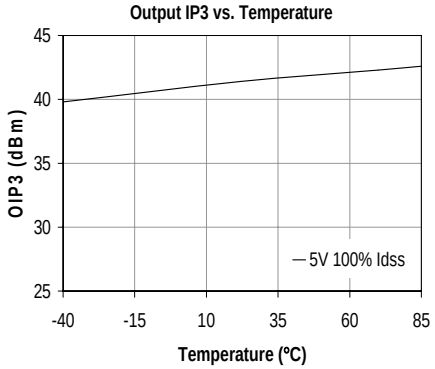
Data is shown at a biasing configuration of $V_{DS}$ = +5 V, $I_{DS}$ = 140 mA, 25 °C for the unmatched device in a 50 ohm system)

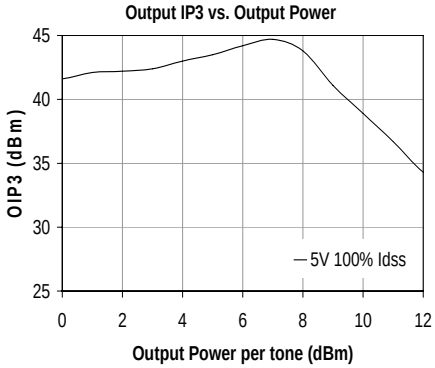


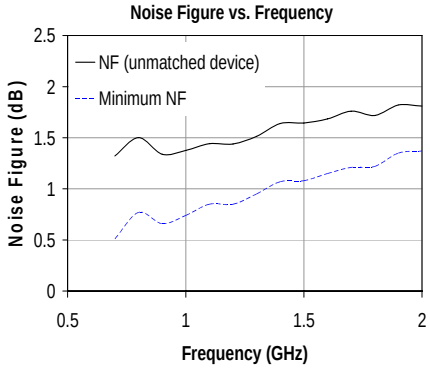




Notes:
The gain for the unmatched device in 50 ohm system is shown as the trace in blue color. For a tuned circuit for a particular frequency, it is expected that actual gain will be higher, as high as the maximum stable gain. The maximum stable gain is shown in the red line. The impedance plots are shown from 10 – 6000 MHz, with markers placed at 0.5 – 6.0 GHz in 0.5 GHz increments.




S-Parameters ($V_D$ = +5 V, $I_D$ = 140 mA, $V_G$ = 0 V, 25 °C, calibrated to device leads)

| Freq (MHz) | S11 (dB) | S11 (ang) | S21 (dB) | S21 (ang) | S12 (dB) | S12 (ang) | S22 (dB) | S22 (ang) |
|---|---|---|---|---|---|---|---|---|
| 50 | 0.00 | -4.08 | 19.36 | 176.06 | -51.05 | 87.96 | -4.38 | -3.34 |
| 250 | -0.13 | -19.64 | 19.19 | 164.65 | -37.15 | 78.37 | -4.52 | -11.51 |
| 500 | -0.34 | -39.41 | 18.85 | 150.19 | -31.34 | 66.75 | -4.77 | -22.43 |
| 750 | -0.55 | -58.33 | 18.47 | 136.21 | -28.24 | 55.74 | -5.19 | -33.05 |
| 1000 | -0.83 | -75.93 | 17.95 | 123.24 | -26.22 | 45.25 | -5.77 | -43.46 |
| 1250 | -1.16 | -93.29 | 17.47 | 110.92 | -24.88 | 35.22 | -6.44 | -53.09 |
| 1500 | -1.50 | -110.36 | 16.82 | 99.18 | -23.95 | 26.69 | -7.14 | -61.08 |
| 1750 | -1.80 | -125.64 | 16.21 | 88.19 | -23.27 | 18.17 | -7.94 | -69.92 |
| 2000 | -2.03 | -140.92 | 15.65 | 77.53 | -22.81 | 9.87 | -8.84 | -78.43 |
| 2250 | -2.25 | -155.64 | 15.05 | 67.15 | -22.39 | 2.11 | -9.57 | -86.41 |
| 2500 | -2.37 | -169.80 | 14.42 | 57.62 | -22.25 | -4.68 | -10.43 | -93.92 |
| 2750 | -2.55 | 177.26 | 13.74 | 48.11 | -22.08 | -11.35 | -11.43 | -101.88 |
| 3000 | -2.62 | 165.93 | 13.18 | 39.86 | -22.01 | -17.16 | -12.30 | -108.95 |

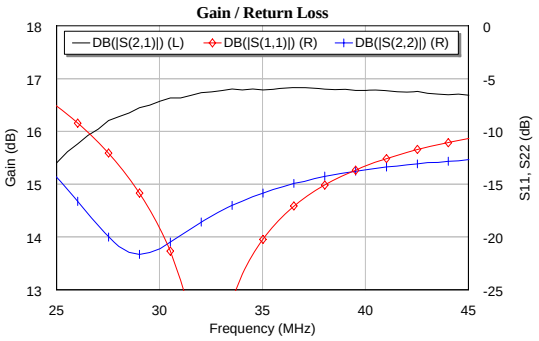
Noise Parameters ($V_D$ = +5 V, $I_D$ = 140 mA, $V_G$ = 0 V, 25 °C, calibrated to device leads)

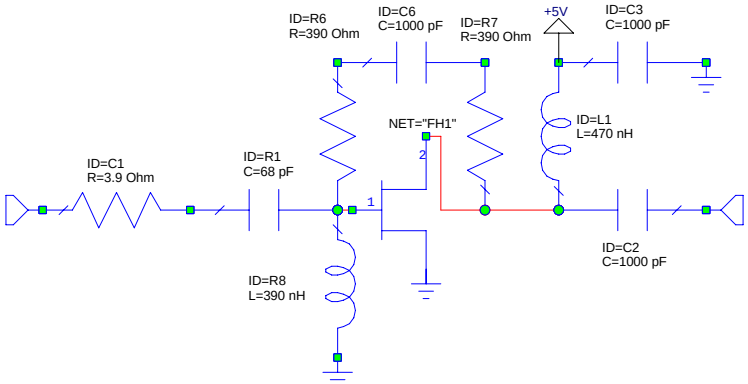
| Freq (MHz) | NF,min (dB) | MagOpt (mag) | AngOpt (deg) | Rn |
|---|---|---|---|---|
| 700 | 0.51 | 0.574 | 32.8 | 0.403 |
| 800 | 0.77 | 0.535 | 37.4 | 0.409 |
| 900 | 0.66 | 0.508 | 44.1 | 0.379 |
| 1000 | 0.74 | 0.488 | 50.4 | 0.365 |
| 1100 | 0.85 | 0.463 | 56.4 | 0.357 |
| 1200 | 0.85 | 0.458 | 62.0 | 0.345 |
| 1300 | 0.95 | 0.446 | 67.3 | 0.335 |
| 1400 | 1.07 | 0.450 | 73.3 | 0.323 |

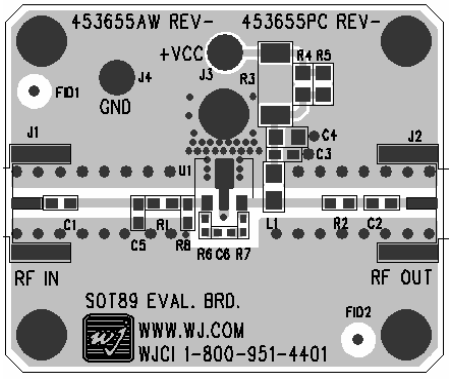
Device S-parameters and noise are available for download off of the website at: http://www.wj.com

# Reference Design: 35 MHz, 17 dB Gain

| Frequency | MHz | 30 | 35 | 40 |
|---|---|---|---|---|
| Gain | dB | 16.6 | 16.8 | 16.8 |
| S11 | dB | -19 | -20 | -13 |
| S22 | dB | -21 | -16 | -14 |
| P1dB | dBm | +21 | | |
| OIP3 | dBm | +39 | | |
| Noise Figure | dB | 4.0 | 3.4 | 3.2 |
| Supply Voltage | V | +5 | | |
| Supply Current | mA | 140 | | |



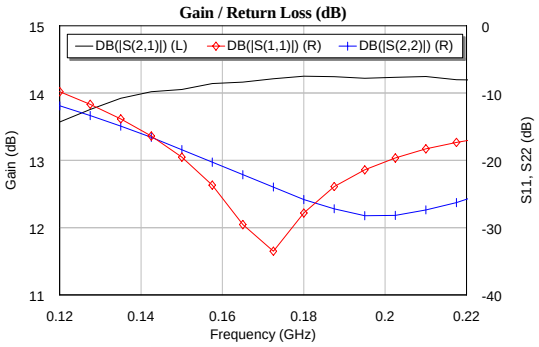



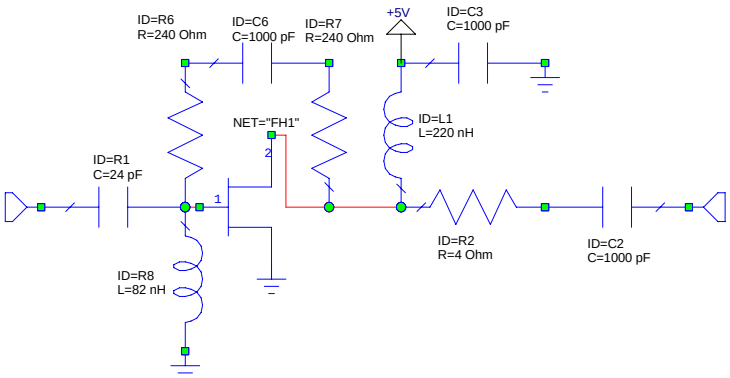



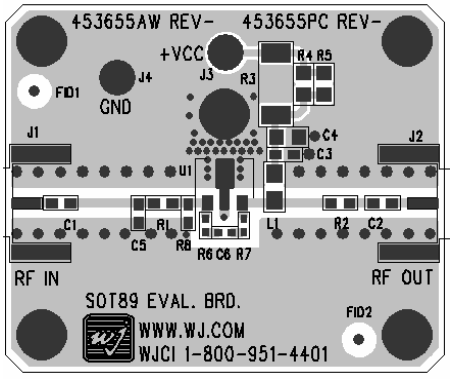

Notes:
1. Circuit Board Material: .014" Getek ML200DSS ($\varepsilon_r$ = 4.2), 1 oz copper. The main microstrip line has a line impedance of 50 Ω.
2. Components not shown in the schematic are either not used or loaded with a thru. Gain for the circuit can be adjusted slightly with the modification of the feedback resistance.

# Reference Design: 170 MHz, 14 dB Gain

| Frequency | MHz | 160 | 170 | 180 |
|---|---|---|---|---|
| Gain | dB | 14.1 | 14.2 | 14.3 |
| S11 | dB | -25 | -33 | -28 |
| S22 | dB | -21 | -23 | -26 |
| P1dB | dBm | +21.6 | | |
| OIP3 | dBm | +42 | | |
| Noise Figure | dB | 2.7 | 2.7 | 2.7 |
| Supply Voltage | V | +5 | | |
| Supply Current | mA | 140 | | |



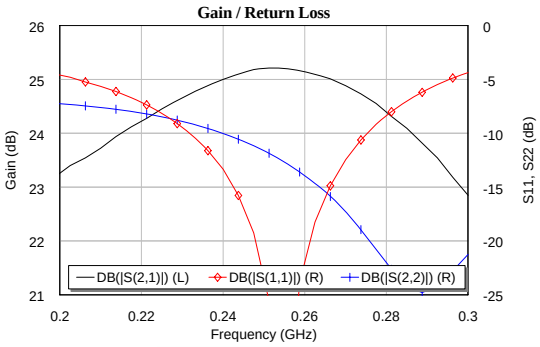



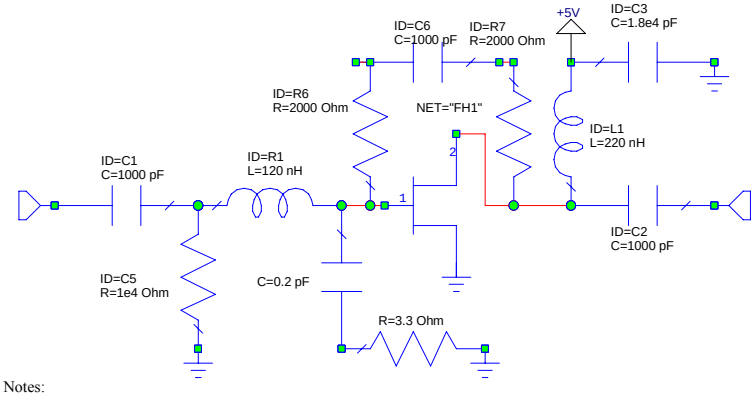

Notes:
1. Circuit Board Material: .014" Getek ML200DSS ($\varepsilon_r$ = 4.2), 1 oz copper. The main microstrip line has a line impedance of 50 Ω.
2. Components not shown in the schematic are either not used or loaded with a thru. Gain for the circuit can be adjusted slightly with the modification of the feedback resistance.

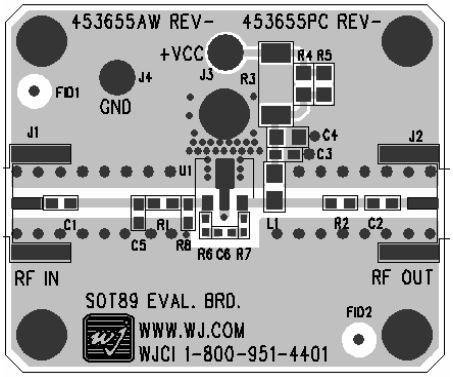
Specifications and information are subject to change without notice.

# Reference Design: 260 MHz, 25 dB Gain

| Frequency | MHz | 250 | 260 | 270 |
|---|---|---|---|---|
| Gain | dB | 25.2 | 25.1 | 24.9 |
| S11 | dB | -23 | -22 | -13 |
| S22 | dB | -12 | -14 | -17 |
| P1dB | dBm | +22.4 | | |
| OIP3 | dBm | +39.5 | | |
| Noise Figure | dB | 1.8 | 1.9 | 2.1 |
| Supply Voltage | V | +5 | | |
| Supply Current | mA | 140 | | |



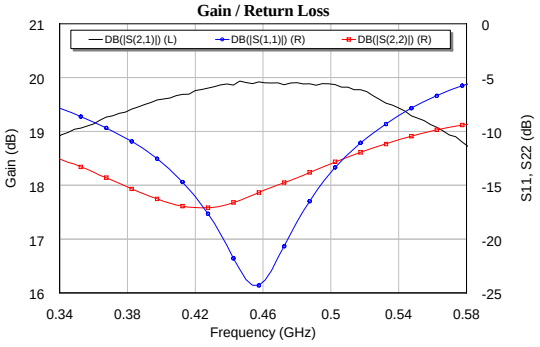



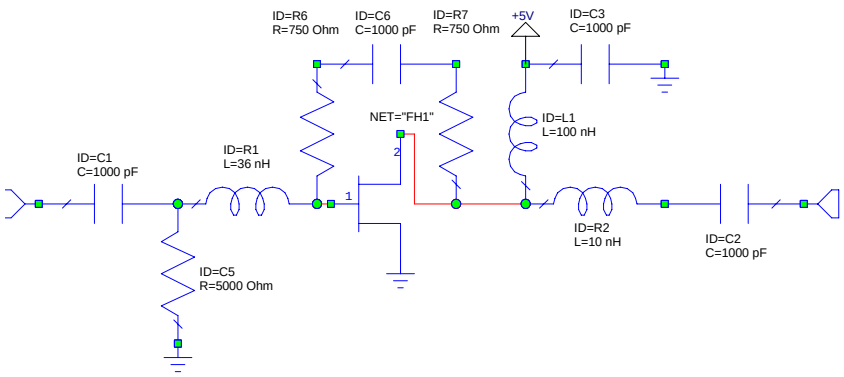



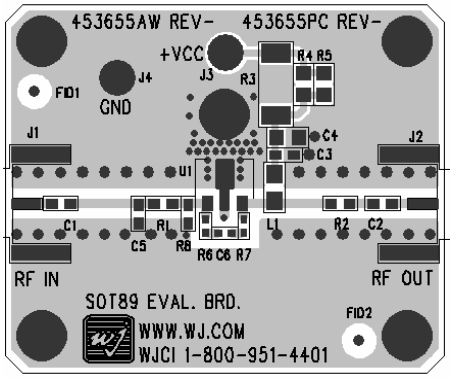

Notes:
1. Circuit Board Material: .014" Getek ML200DSS ($\varepsilon_r$ = 4.2), 1 oz copper. The main microstrip line has a line impedance of 50 Ω.
2. Components not shown in the schematic are either not used or loaded with a thru. Gain for the circuit can be adjusted slightly with the modification of the feedback resistance.

# Reference Design: 460 MHz, 20 dB Gain

| Frequency | MHz | 450 | 460 | 470 |
|---|---|---|---|---|
| Gain | dB | 19.9 | 19.9 | 19.9 |
| S11 | dB | -24 | -24 | -21 |
| S22 | dB | -16 | -15 | -15 |
| P1dB | dBm | +21.6 | | |
| OIP3 | dBm | +42 | | |
| Noise Figure | dB | 1.95 | 2.08 | 2.17 |
| Supply Voltage | V | +5 | | |
| Supply Current | mA | 140 | | |



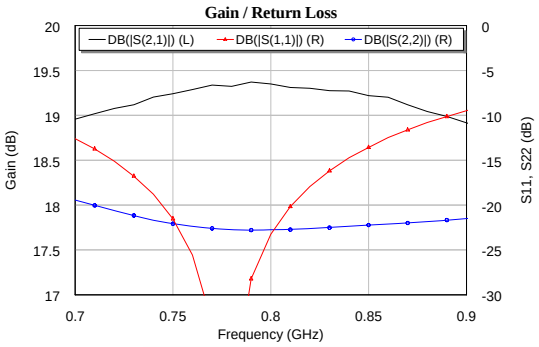



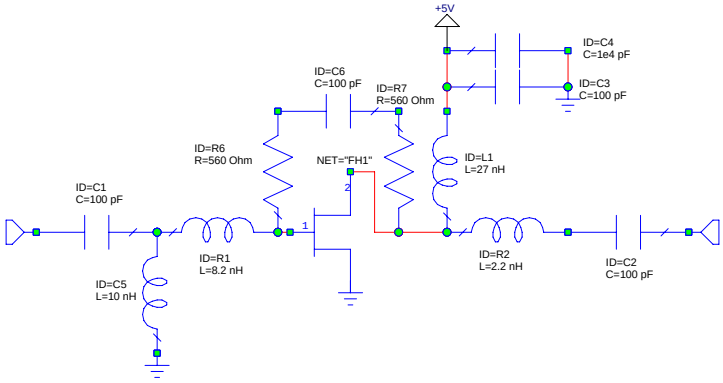

Notes:
1. Circuit Board Material: .014" Getek ML200DSS ($\varepsilon_r$ = 4.2), 1 oz copper. The main microstrip line has a line impedance of 50 Ω.
2. Components not shown in the schematic are either not used or loaded with a thru. Gain for the circuit can be adjusted slightly with the modification of the feedback resistance.

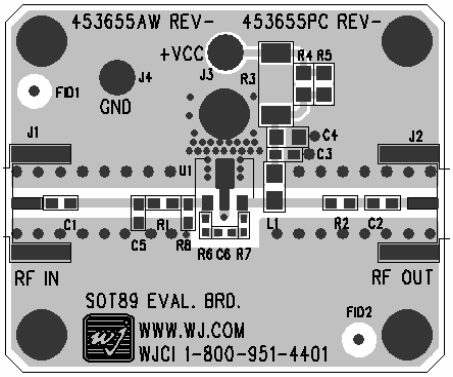
Specifications and information are subject to change without notice.

# Reference Design: 790 MHz, 19 dB Gain

| Frequency | GHz | 746 | 790 | 835 |
|---|---|---|---|---|
| Gain | dB | 19.2 | 19.4 | 19.3 |
| S11 | dB | -20 | -28 | -15 |
| S22 | dB | -22 | -23 | -22 |
| P1dB | dBm | +22 | | |
| OIP3 | dBm | +41 | | |
| Noise Figure | dB | 2.3 | | |
| Supply Voltage | V | +5 | | |
| Supply Current | mA | 140 | | |



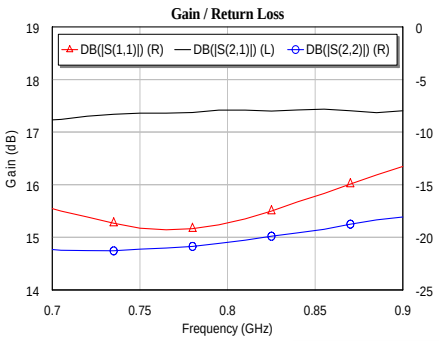



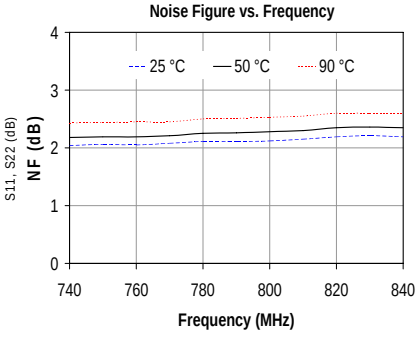



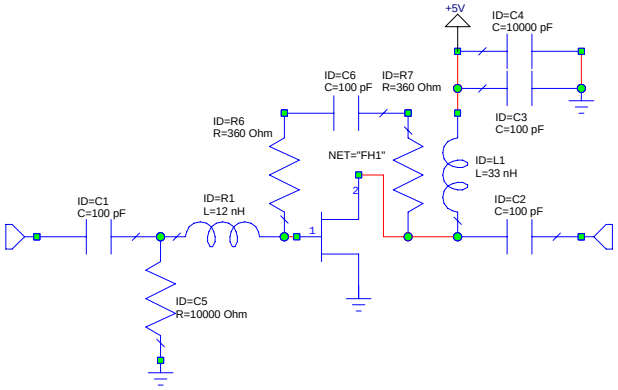

Notes:
1. Circuit Board Material: .014" Getek ML200DSS (εr = 4.2), 1 oz copper. The main microstrip line has a line impedance of 50 Ω.
2. Components not shown in the schematic are either not used or loaded with a thru. Gain for the circuit can be adjusted slightly with the modification of the feedback resistance.

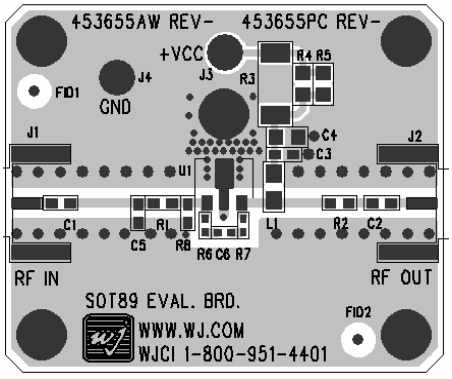
# Reference Design: 790 MHz, 17 dB Gain

| Frequency | GHz | 746 | 790 | 835 |
|---|---|---|---|---|
| Gain | dB | 17.3 | 17.4 | 17.4 |
| S11 | dB | -19 | -19 | -16 |
| S22 | dB | -22 | -22 | -21 |
| P1dB | dBm | +22 | | |
| OIP3 | dBm | +41 | | |
| Noise Figure | dB | 2.0 | 2.1 | 2.2 |
| Voltage | V | +5 | | |
| Current | mA | 140 | | |



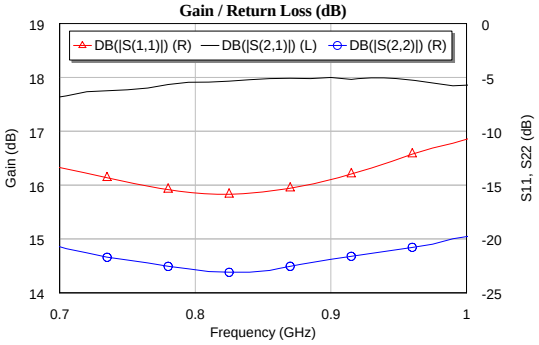



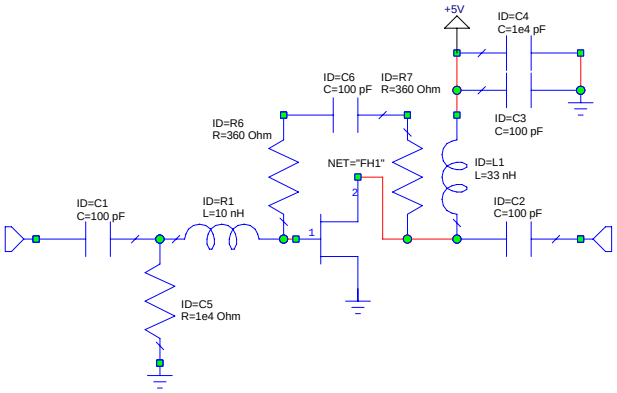

Notes:
1. Circuit Board Material: .014" Getek ML200DSS (εr = 4.2), 1 oz copper. The main microstrip line has a line impedance of 50 Ω.
2. Components not shown in the schematic are either not used or loaded with a thru. Gain for the circuit can be adjusted slightly with the modification of the feedback resistance.

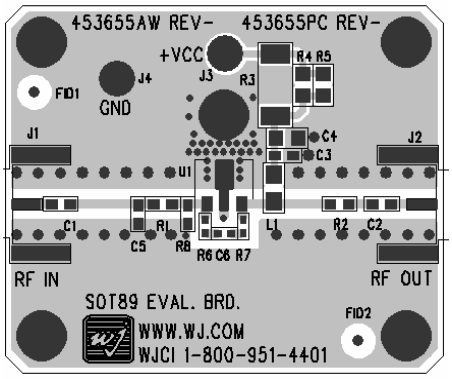
Specifications and information are subject to change without notice.

# Reference Design: 880 MHz, 18 dB Gain

| Frequency | GHz | 850 | 875 | 900 |
|---|---|---|---|---|
| Gain | dB | 17.95 | 17.96 | 18.00 |
| S11 | dB | -16 | -15 | -15 |
| S22 | dB | -23 | -22 | -22 |
| P1dB | dBm | +22 | | |
| OIP3 | dBm | +41 | | |
| Noise Figure | dB | 1.8 | 1.83 | 1.85 |
| Supply Voltage | V | +5 | | |
| Supply Current | mA | 140 | | |



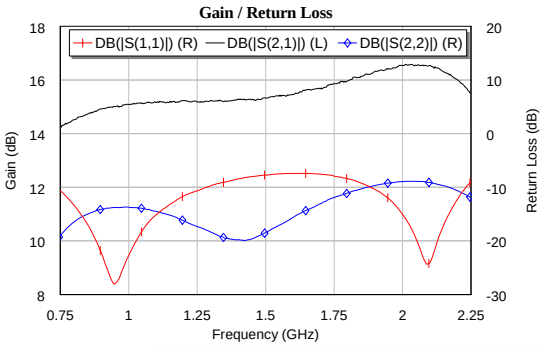



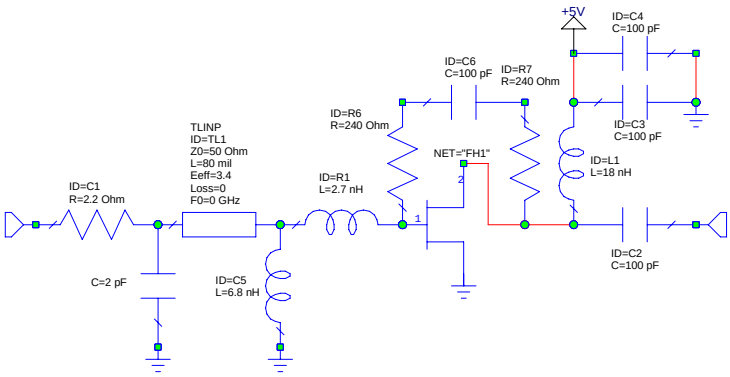



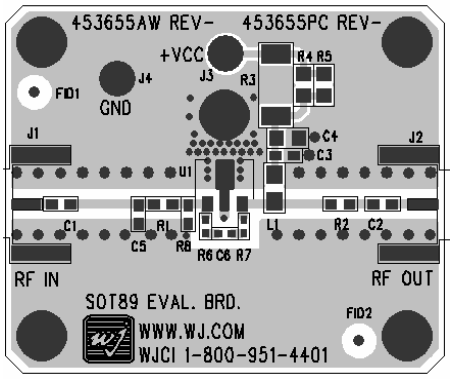

Notes:
1. Circuit Board Material: .014" Getek ML200DSS (εr = 4.2), 1 oz copper. The main microstrip line has a line impedance of 50 Ω.
2. Components not shown in the schematic are either not used or loaded with a thru. Gain for the circuit can be adjusted slightly with the modification of the feedback resistance.

# Reference Design: 800 - 2200 MHz, 15 dB Gain

| Frequency | GHz | 900 | 1900 | 2140 |
|---|---|---|---|---|
| Gain | dB | 14.9 | 16.3 | 16.4 |
| S11 | dB | -22 | -10 | -18 |
| S22 | dB | -14 | -9.7 | -9.6 |
| P1dB | dBm | +22.1 | +22.4 | +22.1 |
| OIP3 | dBm | +40.7 | +42.0 | +41.0 |
| Noise Figure | dB | 2.4 | 2.6 | 2.8 |
| Supply Voltage | V | +5 | | |
| Supply Current | mA | 140 | | |



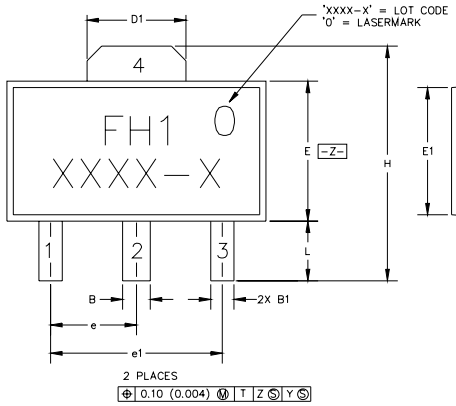

Notes:
1. Circuit Board Material: .014" Getek ML200DSS (εr = 4.2), 1 oz copper. The main microstrip line has a line impedance of 50 Ω.
2. Components not shown in the schematic are either not used or loaded with a thru. Gain for the circuit can be adjusted slightly with the modification of the feedback resistance.
3. A dc blocking capacitor needs to be placed before C1 if dc is present at the input of the circuit.

Specifications and information are subject to change without notice.

# FH1 (SOT-89 Package) Mechanical Information

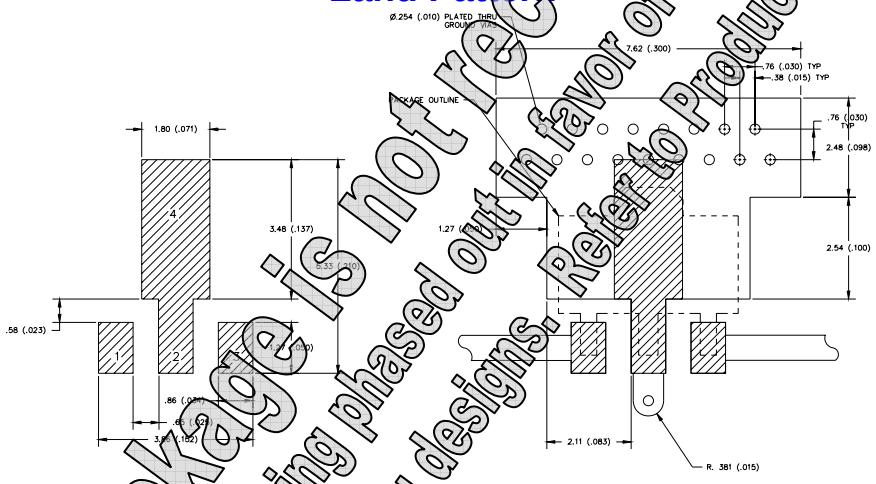
This package may contain lead-bearing materials. The plating material on the leads is SnPb.

## Outline Drawing




| SYMBOL | MIN | MAX |
|---|---|---|
| A | 1.40 (.055) | 1.60 (.063) |
| B | .44 (.017) | .56 (.022) |
| B1 | .36 (.014) | .48 (.019) |
| C | .35 (.014) | .44 (.017) |
| D | 4.40 (.173) | 4.60 (.181) |
| D1 | 1.62 (.064) | 1.83 (.072) |
| E | 2.29 (.090) | 2.60 (.102) |
| E1 | 2.01 (.079) | 2.29 (.090) |
| e | 1.50 BSC (.059) | |
| e1 | 3.00 BSC (.118) | |
| H | 3.94 (.155) | 4.25 (.167) |
| L | .89 (.035) | 1.20 (.047) |
| M | 4.04 (.159) | 4.25 (.167) |

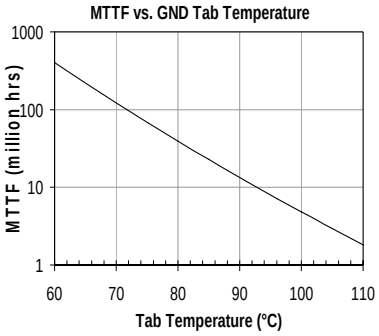
## Land Pattern




## Thermal Specifications

| Parameter | Rating |
|---|---|
| Operating Case Temperature | -40 to +85 °C |
| Thermal Resistance, Rth (1) | 59 °C / W |
| Junction Temperature, Tj (2) | 126 °C |

1. The thermal resistance is referenced from the hottest part of the junction to the ground tab (pin 4).
2. This corresponds to the typical biasing condition of +5V, 140 mA, and an 85°C case temperature. A minimum MTTF of 1 million hours is achieved for junction temperatures below 160 °C.




## Product Marking

The FH1 will be marked with an "FH1" designator. An alphanumeric lot code ("XXXX-X") is also marked below the part designator on the top surface of the package. A "0" will be laser marked in the upper right-hand corner.

Tape and reel specifications for this part are located on the website in the "Application Notes" section.

## MSL / ESD Rating

**Caution!** ESD sensitive device.

ESD Rating: Class 1B
Value: Passes ≥ 500V to <1000V
Test: Human Body Model (HBM)
Standard: JEDEC Standard JESD22-A114

ESD Rating: Class IV
Value: Passes ≥ 1000V to <2000V
Test: Charged Device Model (CDM)
Standard: JEDEC Standard JESD22-C101

MSL Rating: Level 3 at +235° C convection reflow
Standard: JEDEC Standard J-STD-020

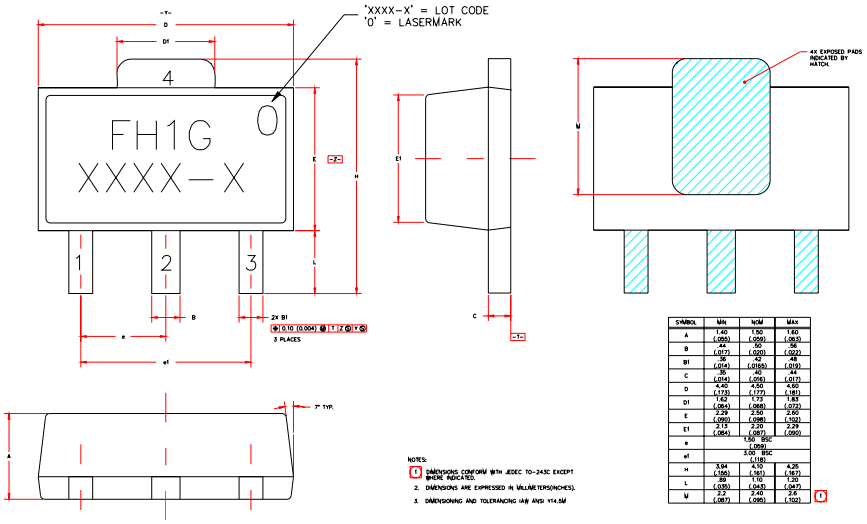
## Mounting Config. Notes

1. Ground / thermal vias are critical for the proper performance of this device. Vias should use a .35mm (#80 / .0135") diameter drill and have a final plated thru diameter of .25 mm (.010").
2. Add as much copper as possible to inner and outer layers near the part to ensure optimal thermal performance.
3. Mounting screws can be added near the part to fasten the board to a heatsink. Ensure that the ground / thermal via region contacts the heatsink.
4. Do not put solder mask on the backside of the PC board in the region where the board contacts the heatsink.
5. RF trace width depends upon the PC board material and construction.
6. Use 1 oz. Copper minimum.
7. All dimensions are in millimeters (inches). Angles are in degrees.

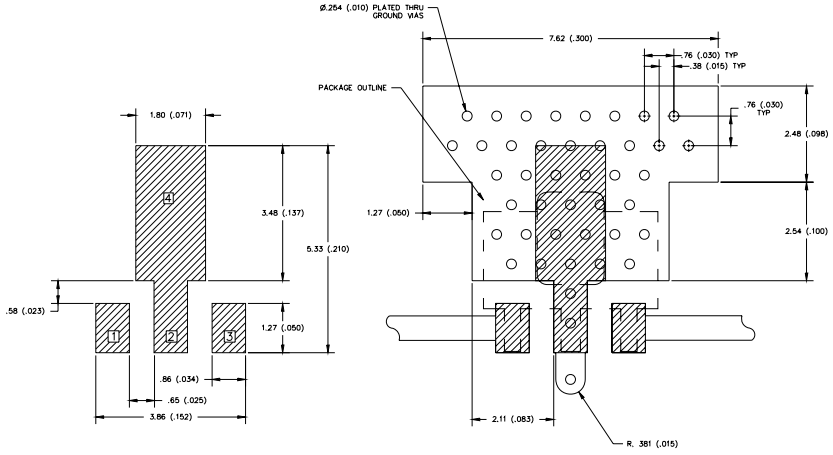
# FH1-G (Green / Lead-free SOT-89 Package) Mechanical Information

This package is lead-free/Green/RoHS-compliant. It is compatible with both lead-free (maximum 260°C reflow temperature) and leaded (maximum 245°C reflow temperature) soldering processes. The plating material on the leads is NiPdAu.

## Outline Drawing




## Land Pattern




## Product Marking

The FH1-G will be marked with an "FH1G" designator. An alphanumeric lot code ("XXXX-X") is also marked below the part designator on the top surface of the package. A "0" will be lasermarked in the upper right-hand corner.

Tape and reel specifications for this part are located on the website in the "Application Notes" section.

## MSL / ESD Rating

**Caution!** ESD sensitive device.

ESD Rating: Class 1B
Value: Passes ≥ 500V to <1000V
Test: Human Body Model (HBM)
Standard: JEDEC Standard JESD22-A114

ESD Rating: Class IV
Value: Passes ≥ 1000V to <2000V
Test: Charged Device Model (CDM)
Standard: JEDEC Standard JESD22-C101

MSL Rating: Level 3 at +260° C convection reflow
Standard: JEDEC Standard J-STD-020

## Mounting Config. Notes

1. Ground / thermal vias are critical for the proper performance of this device. Vias should use a .35mm (#80 / .0135") diameter drill and have a final plated thru diameter of .25 mm (.010").
2. Add as much copper as possible to inner and outer layers near the part to ensure optimal thermal performance.
3. Mounting screws can be added near the part to fasten the board to a heatsink. Ensure that the ground / thermal via region contacts the heatsink.
4. Do not put solder mask on the backside of the PC board in the region where the board contacts the heatsink.
5. RF trace width depends upon the PC board material and construction.
6. Use 1 oz. Copper minimum.
7. All dimensions are in millimeters (inches). Angles are in degrees.

## Thermal Specifications

| Parameter | Rating |
|---|---|
| Operating Case Temperature | -40 to +85 °C |
| Thermal Resistance, Rth (1) | 59 °C / W |
| Junction Temperature, Tjc (2) | 126 °C |

1. The thermal resistance is referenced from the hottest part of the junction to the ground tab (pin 4).
2. This corresponds to the typical biasing condition of +5V, 140 mA at an 85°C case temperature. A minimum MTTF of 1 million hours is achieved for junction temperatures below 160 °C.